A 200 Stages Bi-directional 2-Phases CCD-on-CMOS Back Side Illuminated Time Delay Integration Image Sensor

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***Abstract*— In this paper we describe the architecture of a TDI test-chip embedding a 5 µm pitch pixel, 200 stages, bi-directional TDI pixel fabricated in a BSI technology. This pixel makes use of a unique CDTI based transfer register. The obtained performances are presented and compared to other state-of-the-art CCD-on-CMOS published works.**

Keywords— Time delay Integration (TDI), CCD-on-CMOS, Back Side Illumination (BSI), Bi-directional, anti-blooming, Modulation transfer function (MTF) Time delay Integration (TDI), CCD-on-CMOS, Back Side Illumination (BSI), Bi-directional, anti-blooming, Modulation transfer function (MTF)

I. INTRODUCTION

A new type of charge transfer registers, based on capacitive deep trench isolation (CDTI), has emerged recently paving the way to new CCD-on-CMOS time delay integration (TDI) sensors [2]. These types of image sensors are mostly used in spaceborne and airborne earth observation applications were the motion of the scene is highly predictable. By using a CCD-like charge transfer register, integration time of the scrolling scene can be increased and so signal to noise ratio (SNR) of the obtained image is drastically increased with limited loss of modulation transfer function (MTF).

We have been using this type of charge transfer register for some years now using front-side illuminated technologies (FSI), this paper focuses on our latest achievements obtained on a test-chip embedding a small-pitch, 200-stages charge transfer register fabricated in backside illumination (BSI) technology.

II. TEST CHIP ARCHITECTURE

A. General test-chip overview

Presented results come from a CREAPYX test-chip [1], embedding a 5 µm pitch, CCD-on-CMOS pixel, staggered to form a 200 stages TDI charge transfer register. Since the aim of this test chip is only to characterize pixel performances, the number of columns is restricted, nevertheless pixel design is compatible with 1-dimensional stitching rules so that very large linear sensors can be manufactured. Pixel array is composed of 50 columns and is subdivided into 13 sub-matrices of various sizes in order to choose the amount of summed TDI stages. Since often it is not possible to modulate the aperture of the optical system, choosing the number of summed TDI stages is an important feature that can be seen as a derivative mean to control integration time in order to avoid pixel saturation.

Four dedicated phase drivers have been designed in order to allow the test chip to operate in both transfer directions at a maximum line rate of 100 kHz. Those drivers are made to operate the charge transfer registers sub-matrices in both directions so that scene scan direction can be chosen but also in order to drain the charges generated in the unused register stages in the direction opposite to so scene scan.

Transfer registers embed at both ends a specific output stage, allowing for correlated double sampling (CDS) and having charge conversion factor (CVF) value is 50 µV/e-, yielding an excellent readout noise figure of 3.6 e- rms. Output stages have an extra non-photosensitive TDI stage that allows non-synchronous readout of multiple TDI arrays.

The output of our test-chip is purely analog, output signals are converted in external16 bits ADCs (commercially available). The test-chip sequencer is programmed thanks to a serial interface. Fig. 1 shows a simplifiedblock diagram of the test-chip.

Pixel array has been partially covered by a backside opaque tungsten shield with a specific pattern that can be used for in-situ MTF measurements as well as for anti-blooming efficiency measurements. Pixel array can be operated in two different modes, classical TDI or fame transfer. The latter is

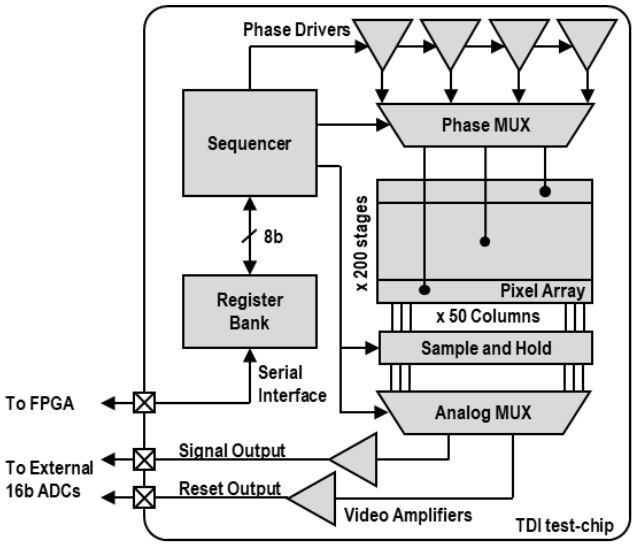

Fig. 1. TDI test-chip block diagram.

mainly used to ease pixel characterization. Fig. 2 shows the layout of the tungsten shield that exhibits slanted edges for MTF measurement purposes and the corresponding image obtained using frame transfer readout.

B. Power concerns

CCD based TDI used to be power-consuming device and the usage of CDTI trenches to mimic CCD behavior was quite troublesome since the capacitance to drive were quite important.

Nevertheless, by choosing an appropriate photodiode doping scheme, we found out that the capacitance operates in a depletion regime most of the time, thus decreasing the apparent capacitance of the trenches and the necessary power to drive them. Accumulation regime is only used to avoid excessive dark current by passivating trenches sidewalls. Going from front side illumination (FSI) to BSI also reduced the CDTI depth, lessening the total power consumption.

Fig. 3 shows a cross-sectional view of a pixel in FSI and in BSI technologies. When going from FSI to BSI, the sensor not only becomes more sensitive to light but power consumption also reduces due to shallower CDTI trenches. There is no noticeable impact on charge transfer efficiency since photodiodes are less deep than CDTI trenches.

Fig. 4 shows a measurement of the CDTI trenches capacitance using a dedicated test structure embedded in the test chip. After reset of the trenches to a negative voltage (V_{reset}), a constant current (I_{cap}) gradually loads the capacitance. Trench capacitance can then be measured thanks to the time derivative of the measured voltage (V_{CDTI}), that is the slope of the obtained curve. One can see that trench capacitance drastically decreases when going from hole accumulation regime ($V_{CDTI} < 0$ V) to depletion regime ($V_{CDTI} > 0$V).

Fig. 5 shows how CDTI trenches are pulsed during charge transfer. Surface state passivation is lost during the transfer pulse since the CDTI are in depletion regime meanwhile. If the pulse lasts for too long, this can contribute to a dark current increase, so it is preferable to minimized that time length. Since CDTI trenches are less capacitive in BSI technology than in FSI, that time length can be minimized in BSI ($t_{BSI} < t_{FSI}$). Presented charge transfer technology has thus remarkably low dark current and as a consequence low readout noise in darkness.

III. Pixel Design

Pixels are designed thanks to the juxtaposition of bi-directional 2-phases charge transfer registers. Actually, pixel transfer registers are made out of 4 phases (2 are longitudinal and 2 are transverse [2]). By choosing an appropriate pair of phases, charges are transferred in one direction or the other.

Fig. 6 shows an electrostatic potential diagram describing how charges are transferred in a first direction when phases 0 and 1 (Φ_0, Φ_1) and respectively phases 2 and 3 (Φ_2, Φ_3) are operated simultaneously. When phases are paired differently, charges will be transferred in the opposite direction.

A specific anti-blooming device has been designed thanks to TCAD simulations and added to the pixel periphery in order to avoid column blooming when pixel array is over-illuminated. Specific collection devices have been added to the pixel in order to enhance charge collection and thus quantum efficiency.

IV. Results

The designed test chip functionality in TDI mode was validated up to a line rate of 100 kHz, nevertheless

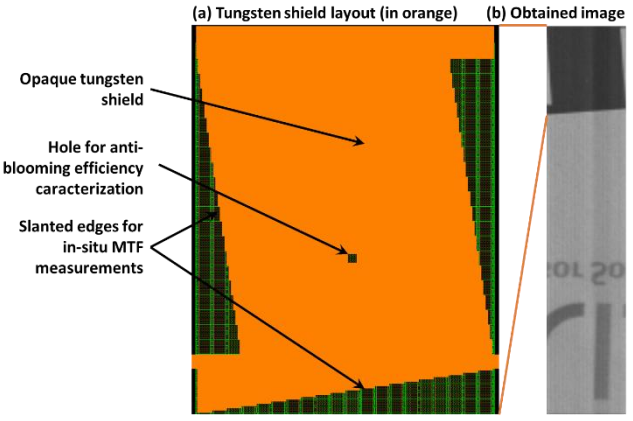

Fig. 2. (a) Backside tungsten shield layout. (b) Obtained image using frame transfer readout.

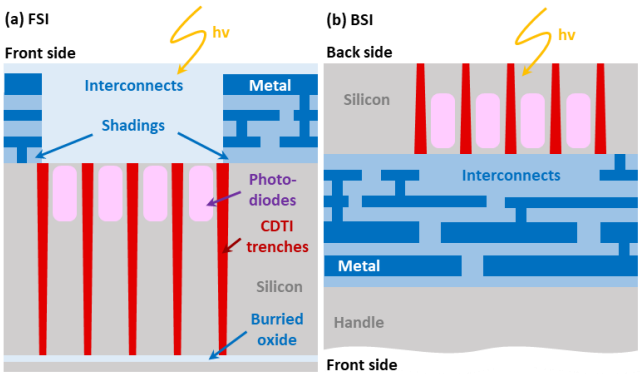

Fig. 3. Cross-sectionnal view of a pixel in FSI (a) and BSI (b).

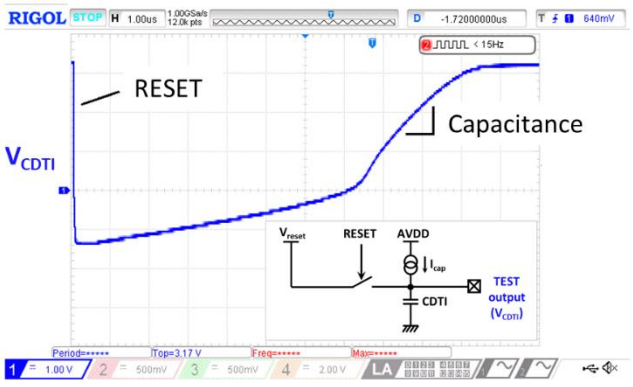

Fig. 4. Measurement of CDTI trenches capacitances.

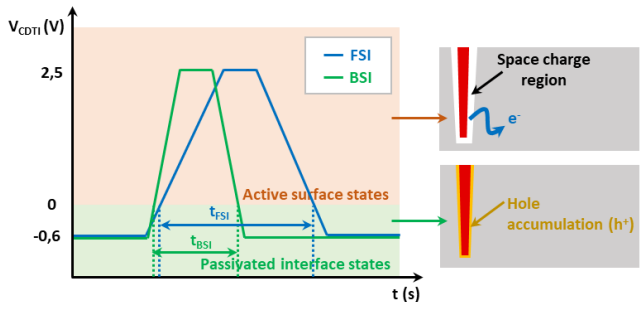

Fig. 5. Trenches sidewall passivation.

performances given here were characterized at a more applicative line rate of 70 kHz.

Fig. 7 shows the obtained mean-variance plot, from which we extract pixel's CVF and linear full well (Qsat) figures. CVF is measured at about 50 µV/e- which yields an outstanding input referred readout noise in darkness of 3.6 e- rms. Linear full well is found at the maximum of the mean-variance at a value of 14.3 ke-. This value is reduced due to the presence of a specific anti-blooming device inside the pixel; no blooming behavior has ever been detected on the detector.

Fig. 8 gives the measured quantum efficiency. Detector shows a peak quantum efficiency of 82% at a wavelength of 530 nm.

Thanks to the use of a BSI technology and reduction of phases pulses duration, our CCD-on-CMOS TDI sensor shows a uniquely low dark current of 3.5 nA/cm² at 60 °C.

Fig. 9 shows how MTF was measured in-situ from previously described backside tungsten light shield pattern. First, pixel data is acquired using frame transfer readout mode

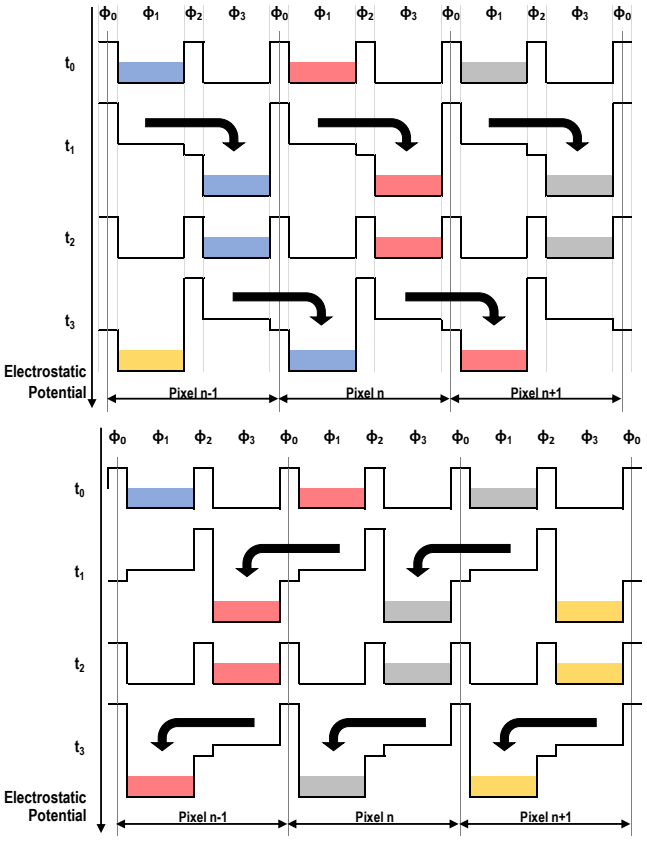

Fig. 6. Electrostatic potential along the register for both transfer directions.

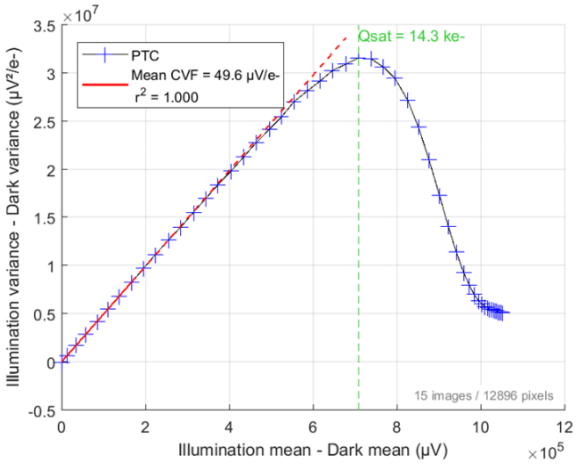

Fig. 7. Mean-variance curve.

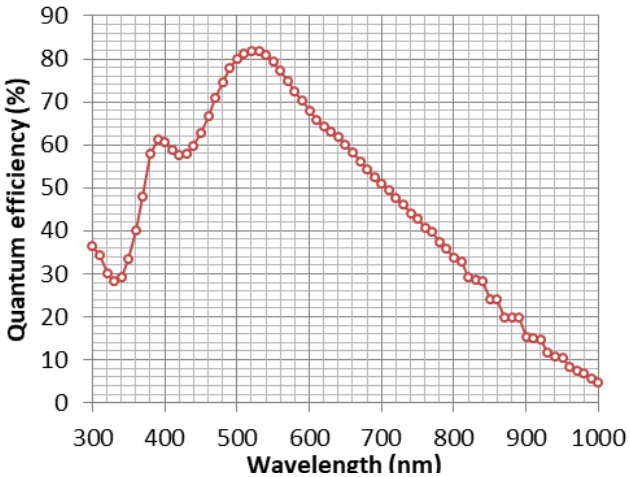

Fig. 8. Measured quantum efficiency.

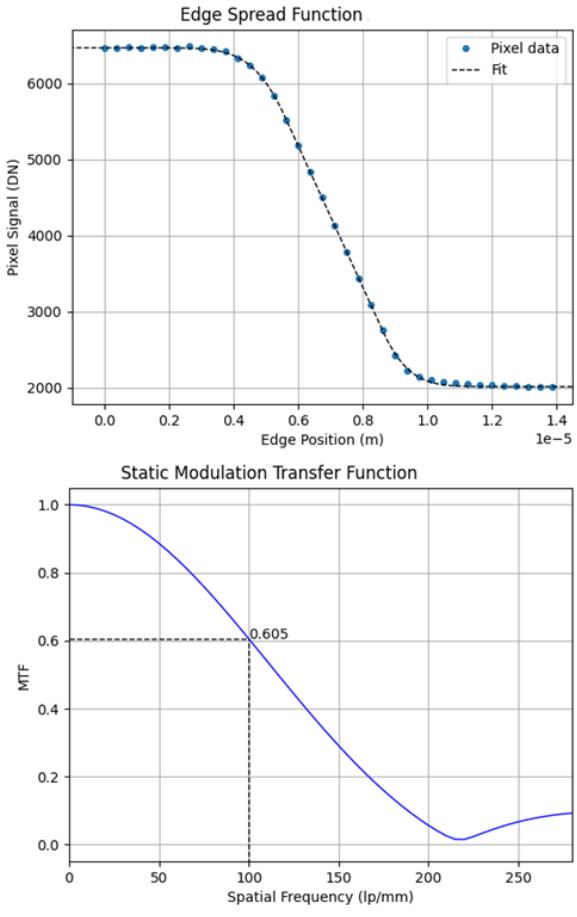

Fig. 9. Edge spead function (top) optained thanks to the tungsten shield and computed MTF curve (bottom).

TABLE I. COMPARATIVE TABLE OF SIMILAR CCD-ON-CMOS IMAGES

	This work	[3]	[4]	[5]	[6]
CCD stages	200	256	192	256	15
Pixel pitch (µm)	5	5.4	3.5	5	5
Pixel architecture	2 phases	4 phases	3 phases	4 phases	4 phases
Row selection	Yes	Yes	Yes	Yes	Yes
Bi-directionnality	Yes	Yes	Yes	Yes	No
Noise in darkness (e- rms)	3.6	10 (HG) 40 (LG)	20	12	12
Linear full well (ke-)	14.3	12.8 (HG) 31.6 (LG)	30	>30	42
CVF (µV/e-)	49.6	62 (HG) 28 (LG)	NA	NA	33
Peak QE (%)	82 (BSI)	89 (BSI)	40.6 (FSI)	53 (FSI)	43
Dark current (nA/cm²)	3.5 (at 60°C)	3.5 (at RT)	3.8 (at 40°C)	3.7 (at 25°C)	NA
Charge transfer inefficiency	< 5.10^{-5}	< 5.10^{-5}	< 5.10^{-4}	< 1.10^{-5}	< 5.10^{-6}
Line rate (kHz)	100	800	58	270	NA
Supply voltage swing (V)	3.1	4.8	NA	NA	NA

and plotted against various positions of this light shield. This data is then fitted in order to obtain a line spread function. Finally, thanks to a Fourier transform, MTF curve is computed. We measured an excellent MTF value of 60.5% at Nyquist frequency. Note that this figure is the static MTF of the pixel and does not include motion blur MTF due to TDI operation, since image was acquired using frame transfer readout mode.

We measured a charge transfer efficiency (CTI) lower than 5.10^{-5}, which is comparable with state-of-the-art CCD-on-CMOS TDI images sensors.

Table I compares our sensor to other similar CCD-on-CMOS published works [3], [4], [5] and [6]. Our work particularly stands out for its low dark current value as well as for its low readout noise. Most papers do not indicate if their TDI image sensor embeds any specific anti-blooming structure. Our TDI is low power thanks to the reduced voltage swing which is applied to the capacitive trenches (-0.6 V to 2.5 V).

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REFERENCES

[1] J. Michelot et al., CNES Workshop on CMOS image sensors for high performance applications. 2015, Toulouse (available on our website www.pyxalis.com).

[2] P. Touron et al., "Capacitive Trench-Based Charge Transfer Device," in IEEE Electron Device Letters, vol. 41, no. 9, pp. 1388-1391, Sept. 2020.

[3] G. Lepage et al., "Time-Delay-Integration Architectures in CMOS Image Sensors," in IEEE Transactions on Electron Devices, vol. 56, no. 11, pp. 2524-2533, Nov. 2009.

[4] David San Segundo Bello et al., "A 7-band CCD-in-CMOS Multispectral TDI Imager," 2017 International Image Sensor Workshop, Hiroshima.

[5] Cheng Ma et al., "Design and Characterization of a 3.5um pitch, 8192 resolution, 5 Spectrum CMOS TDI image sensor," 2017 International Image Sensor Workshop, Hiroshima.

[6] Hyun Jung Lee et al., "Charge-Coupled CMOS TDI Imager," 2017 International Image Sensor Workshop, Hiroshima.