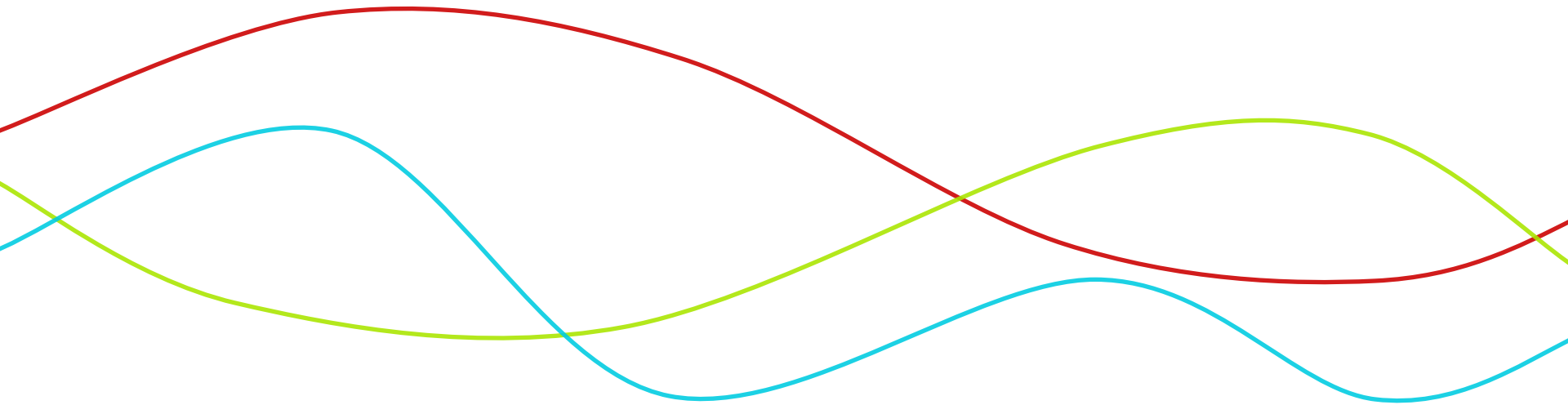


Effects of Transfer Gate Spill Back in Low Light High Performances CMOS Image Sensors



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- VRST Impact on Mean-Variance plot
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Conversion Factor (CVF)

➤ Two definitions of conversion factor (CVF) exist:

❑ Native CVF

$$CVF_{nat} = \frac{dV_{SN}}{dQ_{SN}} \text{ in } \frac{\mu V}{e^-}$$

$$\text{Since } dQ_{SN} = C_{SN} \cdot dV_{SN} \rightarrow CVF_{nat} = \frac{1}{C_{SN}}$$

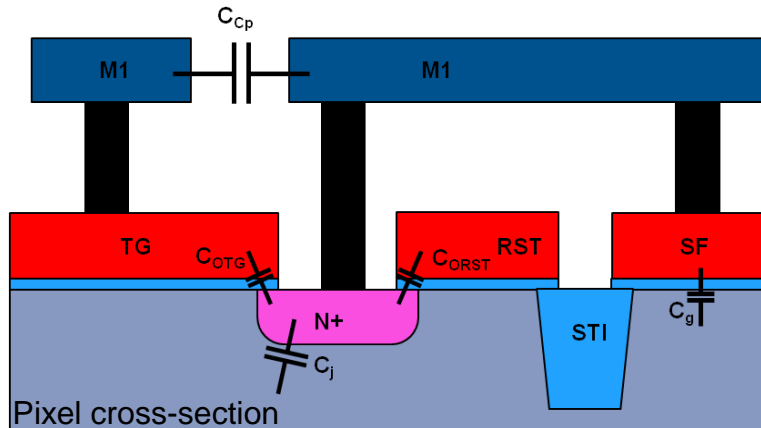
Where : V_{SN} Voltage on the sensing node (SN)

Q_{SN} Total amount of charges on the sensing node (SN)

C_{SN} Total sensing node capacity

$$C_{SN} = C_{Cp} + C_{OTG} + C_{ORST} + C_j + C_g$$

Hypothesis: C_{SN} does not vary with V_{SN} (almost true)



Native CVF measurement is a measurement of the SN capacitance

Conversion Factor (CVF)

Column CVF

$$CVF_{col} = \frac{dV_{col}}{dQ_{SN}} \text{ in } \frac{\mu V}{e^-}$$

$$\text{Since } V_{col} = \gamma \cdot V_{SN} \rightarrow CVF_{col} = \gamma \cdot CVF_{nat} = \frac{\gamma}{C_{SN}}$$

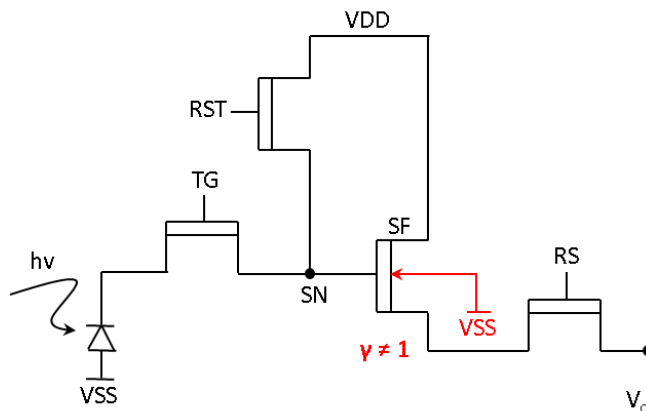
Where : V_{col} Voltage on the pixel column

γ pixel gain (only valid for APS)

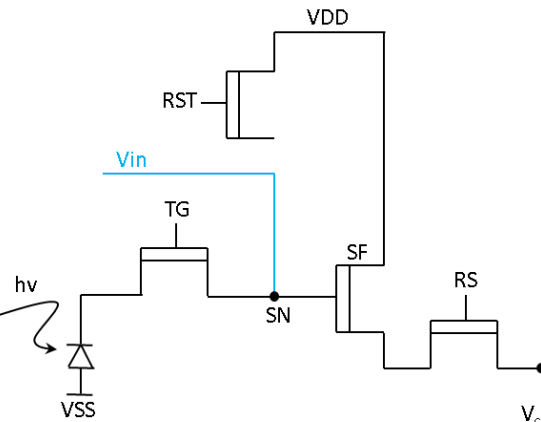
Hypothesis: γ does not vary with V_{SN} (almost true)

γ is in general not equal to one since source follower (SF) bulk is not connected to transistor source \rightarrow would necessitate a well isolation inside pixel array

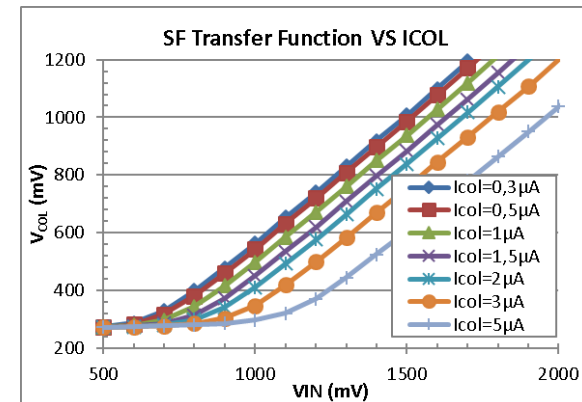
Classical 4T pixel architecture



Modified 4T pixel architecture for gain measurement (minor layout modifications)



Here $\gamma \approx 0.9$



Extraction Method



- Most used method to extract CVF is Mean-Variance plot aka photon transfer curve method ¹

$$V_{col} = CVF \cdot Q_{SN} + V_{off}$$
$$\sigma_{col}^2 = CVF^2 \cdot \sigma_{SN}^2 + \sigma_{off}^2$$

Since e- photo-generation is a Poisson process:

$$\sigma_{e^-}^2 = N_{e^-}$$

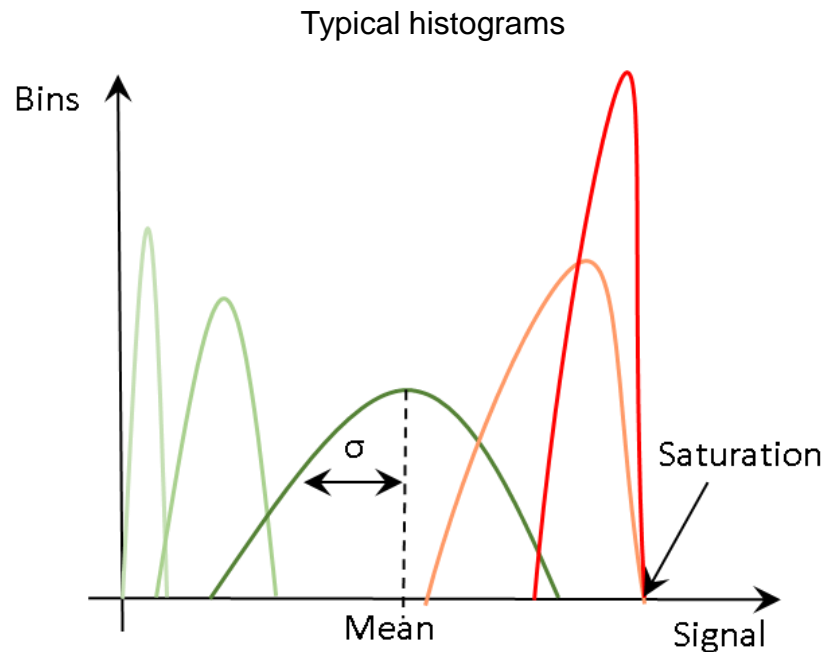
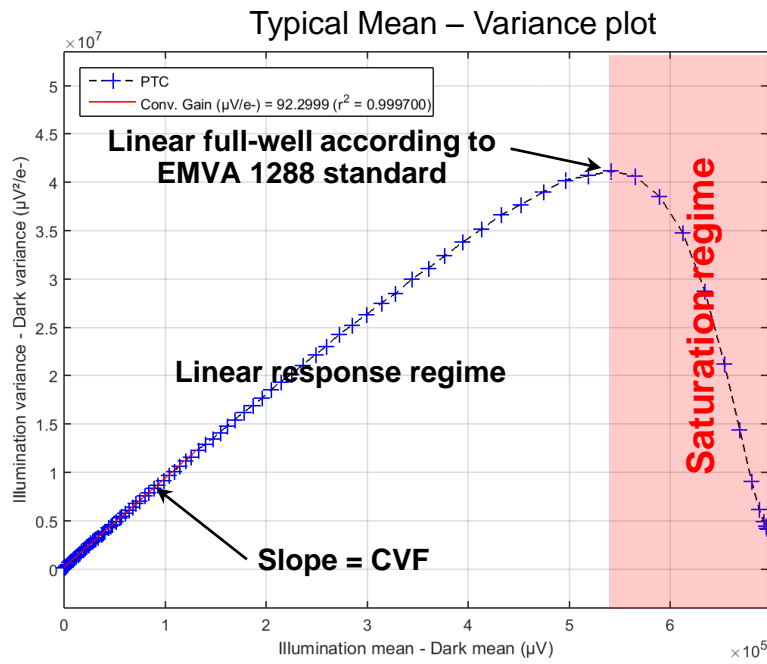
$$\text{Thus } CVF = \frac{d(\sigma_{col}^2 - \sigma_{off}^2)}{d(V_{col} - V_{off})}$$

Where: V_{off} and σ_{off}^2 are the offset voltage and variance on the pixel column
 Q_{SN} and σ_{SN}^2 are the charge and charge variance in the SN
 V_{col} and σ_{col}^2 are the column voltage and variance on the pixel column

¹ Bedabrata Pain and Bruce R. Hancock, "Accurate estimation of conversion gain and quantum efficiency in CMOS imagers", Proc. SPIE 5017, Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications IV, 94 (May 14, 2003);

Extraction Method

- Typical Mean – Variance plots exhibit 2 regimes
 - ❑ Linear response regime
 - ❑ Saturation regime
- CVF is measured in the linear response regime
- According to EMVA 1288 standard² linear full-well can be obtained from maximum of Mean Variance plot (regime transition)

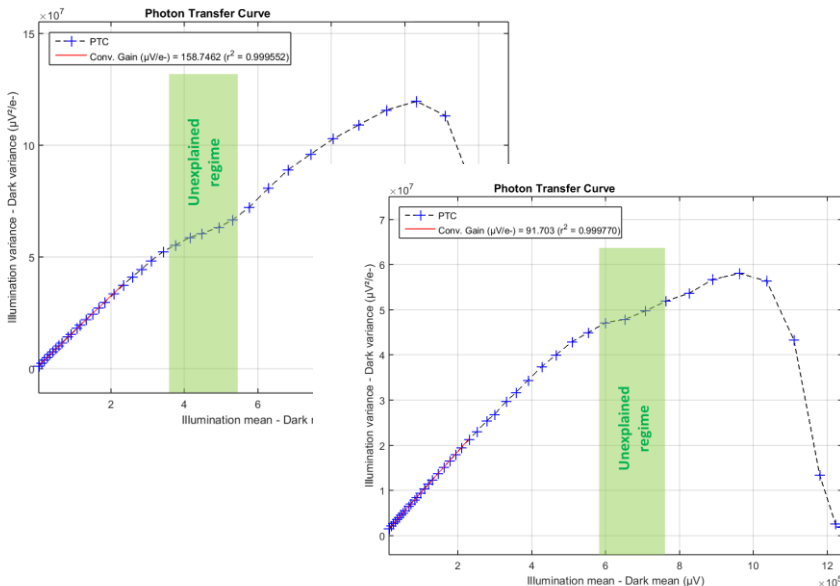


² www.emva.org

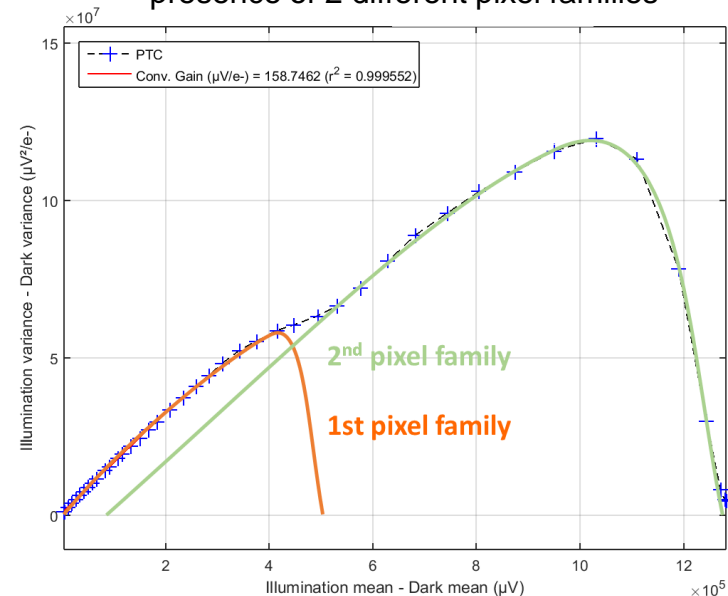
Unexplained Phenomenon

- Sometimes Mean-Variance plots show an unexplained phenomenon
 - ❑ Effects shows up earlier when CVF is high
- A first possible explanation is the presence of two different pixel families
 - ❑ Different full-wells
 - ❑ Different CVF ? (looks like curves are only shifted)
- Other observed effects are lack of linearity in the unexplained regime

Mean – Variance plots with unexplained phenomenon



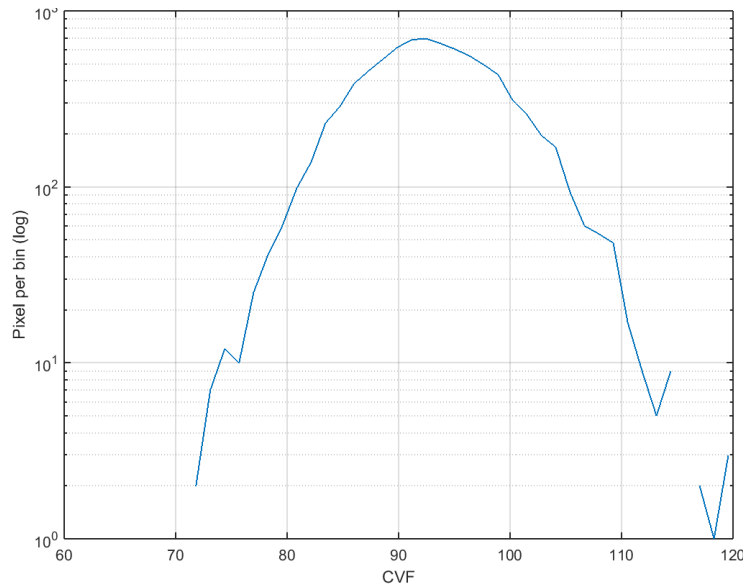
First possible explanation is the presence of 2 different pixel families



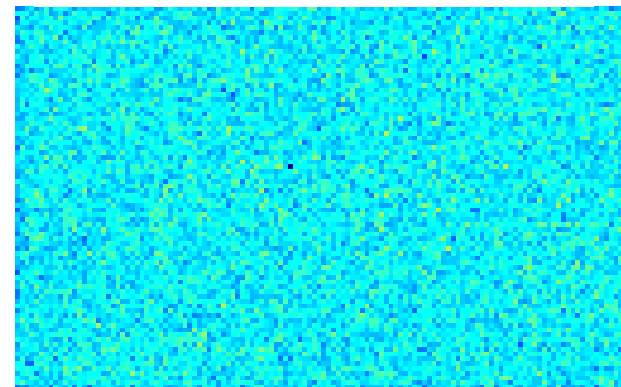
Investigations

- CVF measurement was first performed on all pixels (assuming ergodicity)
 - ❑ First idea is to perform CVF measurements on individual pixels
- Further investigations (pixel CVF) show that
 - ❑ Pixel response looks quite uniform
 - ❑ CVF is evenly distributed (no outliers)
- Statistical effects ?
 - ❑ What about transfer gate spill back (charge partitioning) ???

CVF histogram

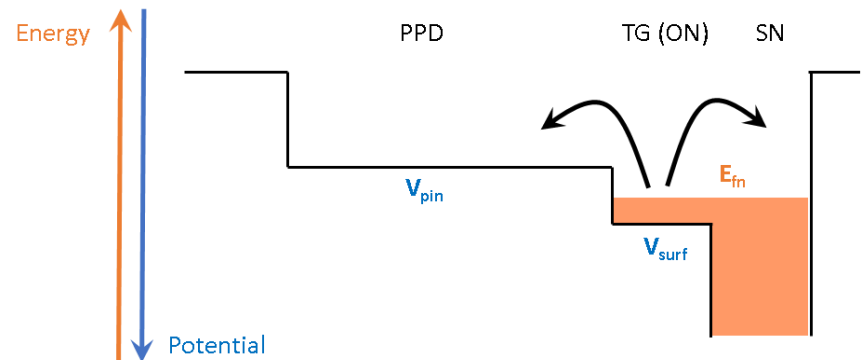


Uniform pixel response



Charge partitioning

- Charge partitioning aka spill-back occurs in pinned photodiodes structures when charges are present under the transfer gate just before being turned OFF
 - ❑ Already undesirable known effect is image lag ³
 - ❑ Only occurs when $E_{Fn} > -q \cdot V_{surf}$ ($V_{SN} < V_{surf}$)
 - ❑ Depends on V_{HITG} (transfer gate voltage when ON) ⁴
 - ❑ Depends on V_{RST} (reset voltage of SN)
- Part of the charges present under the transfer gate will go back into the pinned photodiode (PPD)
 - ❑ Lack of charges in the SN

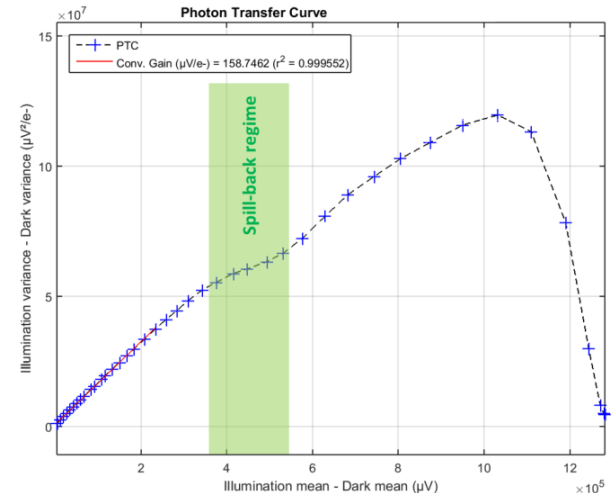
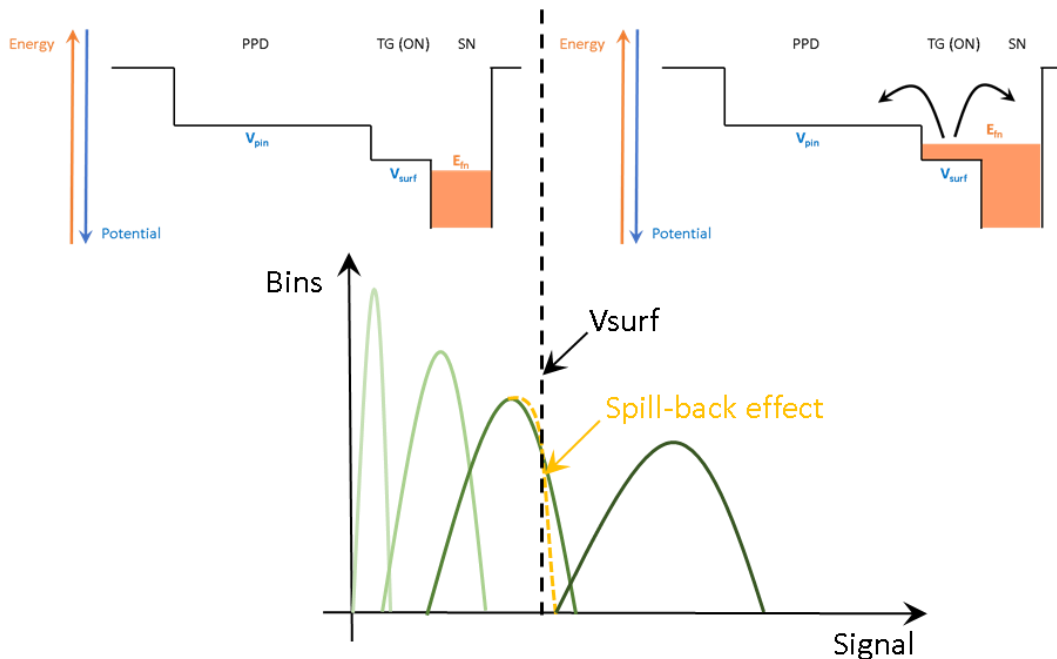


³ L. E. Bonjour, N. Blanc and M. Kayal, "Experimental Analysis of Lag Sources in Pinned Photodiodes," in IEEE Electron Device Letters, vol. 33, no. 12, pp. 1735-1737, Dec. 2012.

⁴ V. Goiffon et al., "Pixel Level Characterization of Pinned Photodiode and Transfer Gate Physical Parameters in CMOS Image Sensors," in IEEE Journal of the Electron Devices Society, vol. 2, no. 4, pp. 65-76, July 2014.

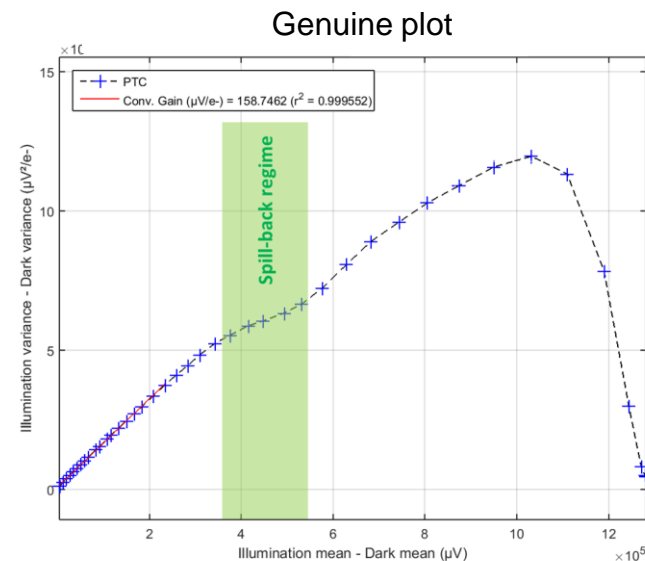
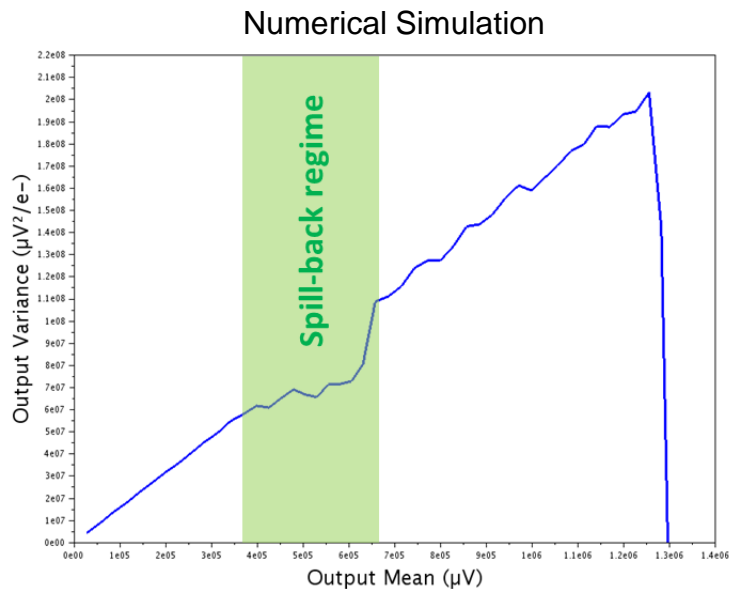
Charge partitioning

- Since charge partitioning only occurs at a given sensing node voltage level (threshold), statistics may be impacted by this phenomenon
 - ❑ Spill back effect only occurs in a part of the measured pixels and modify the statistic (mean, variance)
 - ❑ Once all pixels suffer from spill-back effect, mean-variance plot recovers its expected appearance (coherent with observations)



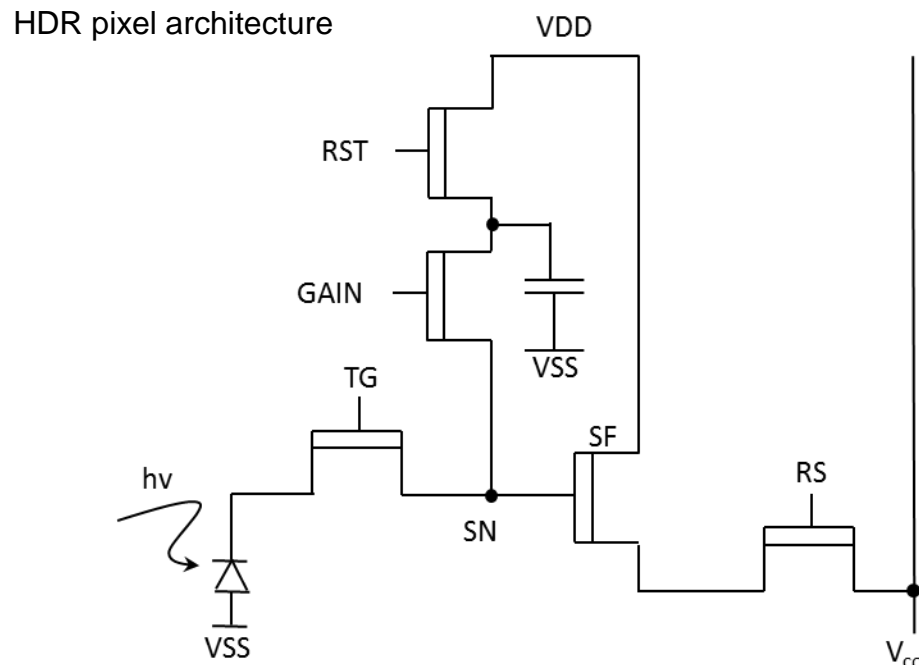
Simulations

- A Mean-Variance plot is drawn thanks to numerical simulations
 - ❑ Pixel data is generated according to a Poisson distribution (300000 points per mean value)
 - ❑ All data points that are above a threshold (equivalent to V_{surf}) are modified
 - ❑ An arbitrary signal is subtracted from the data point in order to emulate the charge loss due to spill back



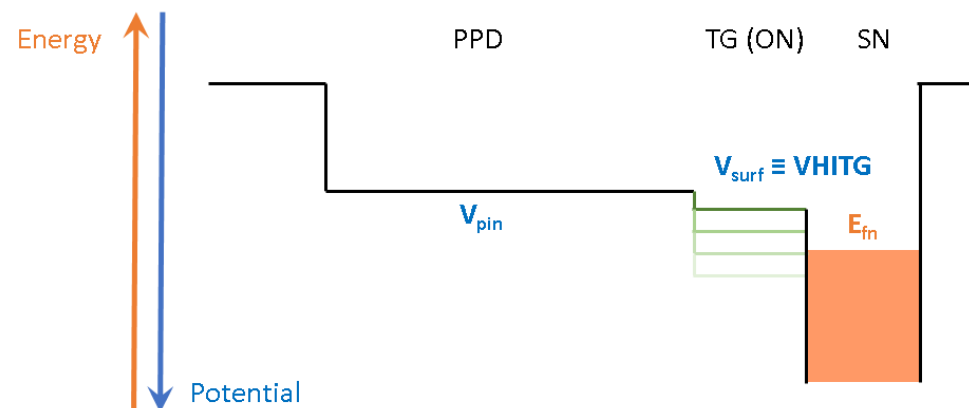
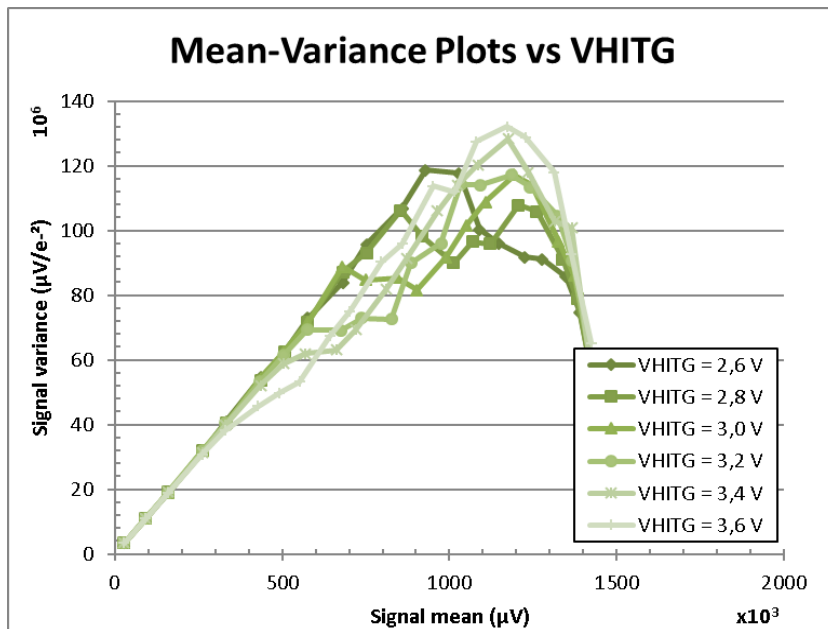
Effects in Low Light CMOS Images Sensors

- Low Light CMOS images sensors need to have low noise
 - ❑ When noise is limited by the in pixel source follower, one way to achieve low noise performances is to have a high CVF
- This effect was observed on HDR pixel architectures
 - ❑ Pixels have an in-pixel capacitor in order to switch pixel CVF.
 - ❑ Spill-back effect was observed in high gain mode (low noise mode)



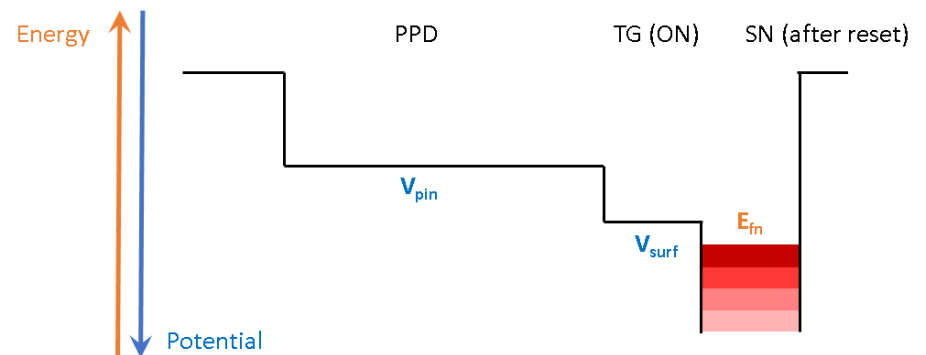
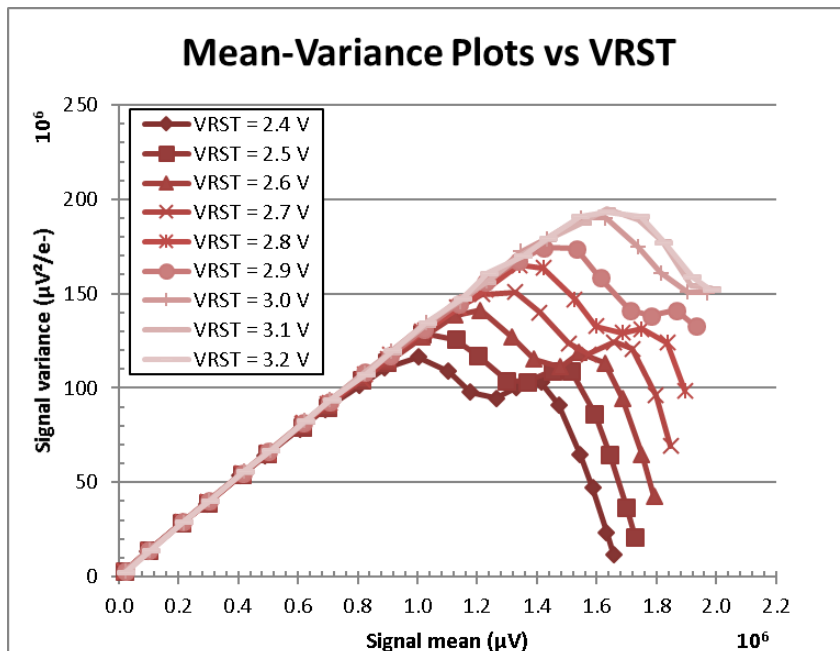
VHITG impact

- Thanks to CREAPYX test chip investigations on VHITG were possible
- VHITG is the voltage of the transfer gate (TG) when ON
- V_{surf} is the channel potential (proportional to VHITG)
- When VHITG decreases spill-back effect occurs for higher signals
 - ❑ Thus pixel remains linear in a higher dynamic range
- A lower VHITG yields better pixel performances



VRST impact

- VRST is the reset voltage of the sensing node (SN)
- Higher VRST allows to push back spill-back effect to higher signal values
- For higher CVF values spill-back effect appears earlier
- Too high VRST values can produce an incorrect reset (soft reset)
 - ❑ The best tradeoff has to be found



Conclusions



- When designing/characterizing low noise pixel architectures one often use high CVF values
 - ❑ Mean-variance plots may then exhibit strange behaviour
 - ❑ Also has an impact on pixel linearity

- Dedicated, flexible test chips (CREAPYX) are always good help to understand undesired phenomena

- This effect seems to be linked to already known spill-back effect
 - ❑ Simulations, VHITG and VRST impact seem to confirm this hypothesis

- VHITG and VRST are two good candidates to alleviate this effect

- Choosing a lower VHITG value, when possible (no lag), allows to push back this effect to higher signal values