Digital integration: a path to lower system cost in imaging systems

Benoit Dupont, Pyxalis, booth 2042
PYXALIS
in a few words...
PYXALIS is a high-end CMOS Image Sensor supplier & Design house

A few figures:
- Founded in: 2010
- Team: 20 people
- Experience: >150 man-year experience in CMOS image sensors

Located in **Grenoble**, France, in the «Imaging Vallée»:
700sqm offices, state of the art design center, full EO characterization
Pyxalis is a custom image sensor supplier in the field of:

- Medical
- Security
- Machine Vision
- Science
- Air and space born applications

With a strong emphasis on **High performance SoCs**
Digital integration, a path to lower total system cost

In consumer image sensor industry, the trend towards more compact systems is undeniable...
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What about industrial application?
What about industrial application?

The trend is also there, slower of course, due to:

- Development cost pressure
- Performance requirements, optical formats, etc…
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Yet, today a significant part of the camera functions can be performed by the imager itself:

- Auto white balance (AWB)
- Auto exposure control (AEC)
- Auto gain control (AGC)
- Edge sharpness enhancement
- Lens vignetting correction
- Color interpolation
- Gamma correction
- RGB to Ycrcb transformation
- Picture statistic

- Defect correction
- Automatic Black clamp/ calibration
- Row and column fixed pattern noise correction
- Stitching artifact corrections
- Binning subsampling,
- Multi ROI,
- Flip H&V and combined modes
- High dynamic range reconstruction
- Image formatting

➡ Smaller, cheaper FPGAs, smaller memories, etc…
Typically, on-chip sequencers are made using hard-coded synthetized logic:

**VHDL CODE**

Synthetizer
We propose a different approach: processor driven digital sequencing.
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But Why?

VHDL CODE

Source CODE

Synthetizer

compiler

Processor core
We propose a different approach: processor driven digital sequencing.

But Why?

- Significant advantages for custom design:
  - Great user flexibility
  - Faster simulation cycles
  - Easier debugging
  - Easier to fix (if required)
  - Easier reuse
  - Overall shorter design cycles
  - Lower design risks
  - Take over more camera functions
Digital integration, a path to lower total system cost

processor driven digital sequencing

- 32bits APS on-chip for maximum flexibility:
- Windowing / subsampling
- Integration time and mode management (ERS, GS, Snapshot, RWI/Overlapp)
- Black level correction, fine digital gains, etc.

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processor driven digital sequencing

- Oriented towards machine vision:
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Technology limited clock rate, but:

- Multiple cores
- Dedicated peripherals
- Application specific cores
Example: Multiple cores

- To run different codes
- Branching and conditions sets by user with SPI
- ROIs, binning, subsampling, etc…
Example: Dedicated Peripherals: HDR reconstruction

Pixel gains (1..n) over 14bits

Real time HDR reconstruction

20bits linear output
Example: in the future, application specific cores:

- Run, modify, update client specific functions
- Uploadable code (SPI, external Eeprom…)
- Allowing camera maker to add value to the camera
Where are the limits to this approach?

- Imaging technology nodes are not state of the art in terms of digital performances

- Best is to combine:
  - an opto technology for the detection area
  - a digital technology node for processing

(Source LETI)
3D Stacking: doing it for the right reason

- Compactness ?
- Performance ?
- Cost ?
- Power ?
- Right trade-off with dual chips solution ?
Thank you!

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